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SAMPA chip: a new ASIC for the ALICE TPC and MCH upgrades

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Abstract: This paper presents the SAMPA, an ASIC designed for the upgrade of read-out front end electronics of the ALICE Time Projection Chamber (TPC) and Muon Chambers (MCH). SAMPA is made in a 130 nm CMOS technology with 1.25 V nominal voltage supply and includes 32 channels, with selectable input polarity, and five possible combinations of shaping time and sensitivity. Each channel comprises a Charge Sensitive Amplifier, a semi-Gaussian shaper and a 10-bit ADC, followed by a Digital Signal Processor. A prototype in a multi project run was submitted to evaluate the performance of each of these blocks. The experimental results of the tests on these building blocks are presented, showing a substantial agreement with requirements.

Keywords: Analogue electronic circuits; Front-end electronics for detector readout

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2016 JINST 11 C02088

Contents

1 Introduction

ALICE (A Large Ion Collider Experiment) is one of the four big experiments at the LHC accelerator. The experiment is devoted to the study of the strongly interacting matter and the quark-gluon plasma at the high energy density and temperature that is achievable in relativistic heavy ion collisions. The present ALICE detector was designed to handle very high multiplicity, and was optimised for that, compromising the capability to run at high rate. The LHC machine will provide, starting from 2020, after its second long shutdown, a higher luminosity, and consequently higher event rate. The scientific plan of ALICE requires to profit of this higher luminosity, therefore an upgrade plan was set. One key point is to upgrade the Time Projection Chamber (TPC), maintaining its present tracking performance, but allowing it to run at 50 kHz event rate. Besides modifying the read-out plan of the detector, the front-end electronics need to be replaced. It was decided to develop a new ASIC, named SAMPA, designed to serve both the TPC and the Muon Chambers [1]. The chip should integrate a pre-amplifier, an ADC and it must have a digital processing capability to provide baseline shift compensation and signal filtering to reduce the data size. The TPC read-out plane is based on Gas Electron Multiplier (GEM) detectors, while the MCH is using Multiwire Proportional Chambers (MWPC). The two detectors have different requirements, and the table 1 shows the main specifications for the two cases.

2 The SAMPA chip

The SAMPA chip has 32 channels and it is composed of an analog front-end part, an ADC and a digital processor, as illustrated in figure 1. It is designed and fabricated in 130 nm TSMC CMOS technology. In the next sections, each of these parts will be discussed.

Table 1. Original specifications of the front-end ASIC (SAMPA).

Specification	**TPC**	**MCH**
Voltage supply	1.25 V	1.25 V
Polarity	Negative	Positive
Detector capacitance (Cd)	18.5 pF	40 pF–80 pF
Peaking time (ts)	160 ns	300 ns
Shaping order	4th	4th
Equivalent Noise Charge (ENC)	< 600e@ts=160 ns*	< 950e @ Cd=40 pF* < 1600e @ Cd=80 pF*
Linear Range	100 fC or 67 fC	500 fC
Sensitivity	20 mV/fC or 30 mV/fC	4 mV/fC
Non-Linearity (CSA + Shaper)	< 1%	< 1%
Crosstalk	< 0.3%@ts=160 ns	< 0.2%@ts=300 ns
ADC effective input range	2 Vpp	2 Vpp
ADC resolution	10-bit	10-bit
Sampling Frequency	10 (20) Msamples/s	10 Msamples/s
INL (ADC)	<0.65 LSB	<0.65 LSB
DNL (ADC)	<0.6 LSB	<0.6 LSB
ENOB (ADC)**	> 9.2-bit	> 9.2-bit
Power consumption (per channel) CSA + Shaper + ADC	< 15 mW	< 15 mW
Channels per chip	32	32

*: R_{esd} = 70Ω

**: @ 0.5MHz, 10Msamples/s

2.1 Analog front-end

The SAMPA front-end is composed by a Charge Sensitive Amplifier (CSA), capable to amplify either positive or negative charge pulses, followed by two shapers and a non-inverting stage. The CSA feedback is composed by a parallel capacitive feedback C_f and a resistive feedback R_f. Then are placed, sequentially, a Pole-Zero Cancellation (PZC) network, a high pass filter, two bridged-T second order low pass filters, a non-inverting stage, as visible on the left side of figure 1. The first shaper is a scaled-down version of the CSA and it generates the first two poles and one zero. A copy of the first shaper, connected in unity gain configuration is implemented in order to provide a differential mode input to the next stage. The second shaper is a fully differential second order bridged-T and it includes a Common-Mode Feed-Back network (CMFB).

The non-inverting stage adapts the DC voltage level of the shaper output to use the full dynamic range of the ADC. It consists of a parallel connection of two equally designed Miller compensated amplifiers and an output RC low pass filter (R=50 Ω, C=20 pF)

The CSA is based on a cascode topology, which was modified to improve the noise figure, providing a relatively flat minimum for the expected detector capacitance value. Full details can be found in [2] and [3]

2016 JINST 11 C02088

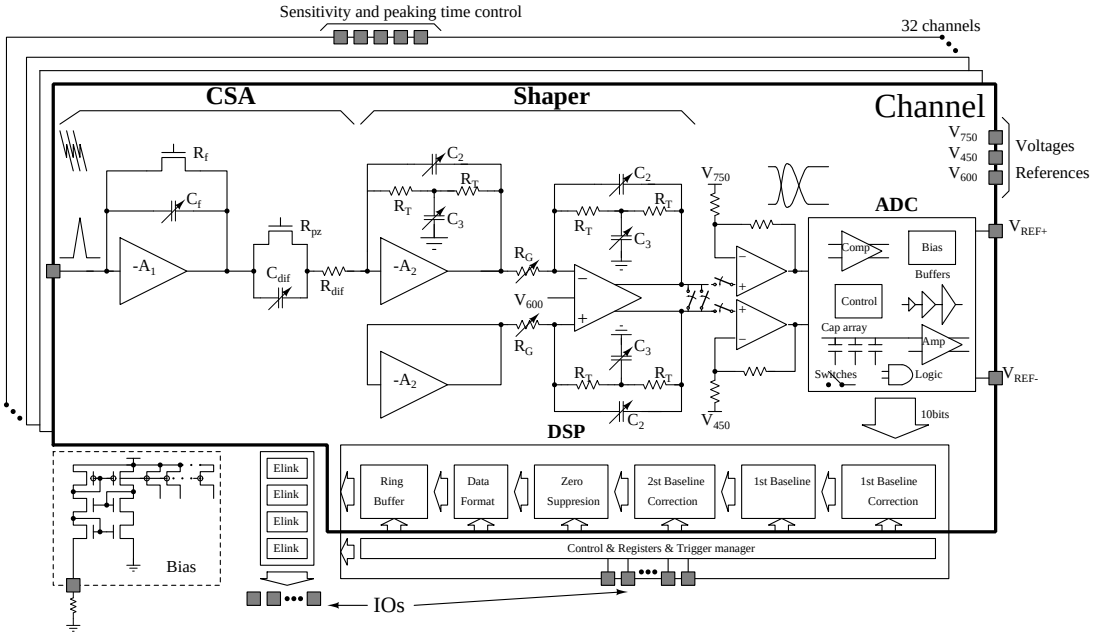

Figure 1. Sampa block diagram.

2.2 The digitisation stage

The SAMPA includes a 10-bit capacitive successive-approximation (SAR) ADC per each channel. It is optimised for operation at 10 MSps, with the capability to be run up to 20 MSps. The ADC implemented a low energy switching technique, based on the merged capacitor switching technique presented in [4].

2.3 Digital Signal Processor

The Digital Signal Processor (DSP) is composed of a set of digital filters, a data compression (zero suppression — ZSU) block, data formatting, buffers and serial output drivers. There are also several blocks controlling the chip operation. The main elements of the DSP are:

- Filters: there are 4 filters implemented in the SAMPA chip: Baseline Correction 1 (BC1), that is responsible to deal with slow variations in the baseline of the signal; Digital Shaper (DS), that aims to reshape the already shaped digitised pulse to minimize the bandwidth; Baseline Correction 2 (BC2) that aims to track and remove fast variations in the baseline; Baseline Correction 3 (BC3), implemented in order to complement and/or substitute the functions of BC1 and BC2 with a more robust approach to track the baseline, using a slope filter.

- Data Format: responsible for adding extra information to the datasets to compensate for the ZSU compression.

- Ring Buffer: stores packets until they are sent out.

- Serial Outs: sends data out from the Ring Buffers, when packets are completed.

2016 JINST 11 C02088

- Event Manager: generates the time window necessary for defining the beginning and end of the packets.
- Pre-samples: accumulates a number of samples so that the chip has access to before-trigger samples (useful for triggered runs only), also known as Trigger delay.
- Clock manager: source of all the divided clock domains.
- Communication: an I2C commercial interface is used to communicate with SAMPA.
- Neighbour ASIC: this feature will be used for the MCH detector, which has more channels but much fewer data rates than the TPC. In this case, some chips may be daisy-chained so that they pass data to each other up to the last on the chain that actually outputs the data.

3 Experimental results

The different blocks composing the SAMPA ASIC were experimental verified in a Multi-Project run. The silicon area available in this run (5x5 mm^2) was divided in 3 mini-chips. The first one (chip_1) contained 5 channels of the front-end block (charge sensitive amplifier + two stages shapers) to investigate sensitivity, noise and cross-talk of the analog block. The second mini-chip (chip_2) was hosting an ADC and a prototype of SLVS drivers. The third minichip (chip_3) was hosting a 3 channel full chain FE+ADC+simplified DSP.

3.1 Characterising the CSA

The chip_1 measures approximately 2x3 mm^2 and was encapsulated in a CQFP64 package. The main performance of the chip were tested by different groups and compared with the simulation. The 1.25 V needed to power the chip was provided directly from an external power supply, while the three external reference voltages used for the buffer (450 mV, 600 mV and 750 mV) were generated on-board. The input charge was generated using a voltage step into a capacitor connected in series with the input. The differential output of the second shaper was analysed by an oscilloscope via a differential probe. Visual inspection of the shape of the pulse (e.g. figure 2) never showed anomalous behaviours, besides an undershoot in the baseline restoration for the high gain (20mV/fC and 30mV/fC) configurations. The pulse amplitude and shaper as a function of the detector capacitance was studied: the shape of the pulse did not change significantly, the amplitude decreased, while the undershoot became more evident.

The measured peaking time resulted systematically shorter than value obtained in simulation, being between 135 ns and 145 ns for the 160 ns nominal configuration, and 245 ns and 260 ns for the 300 ns nominal configuration.

The sensitivity and linearity of the front-end was evaluated by performing a complete scan of the dynamic range, taking also a few points in the saturation zone. For each injected charge value were collected about one thousand waveforms. On each waveform, the amplitude of the maximum value of the peak was computed with the oscilloscope function, then the average values among all the collected waveforms was taken. A waveform for each injected charge values was saved and, for a few cases, an offline analysis involving fitting the output pulse was performed, providing

2016 JINST 11 C02088

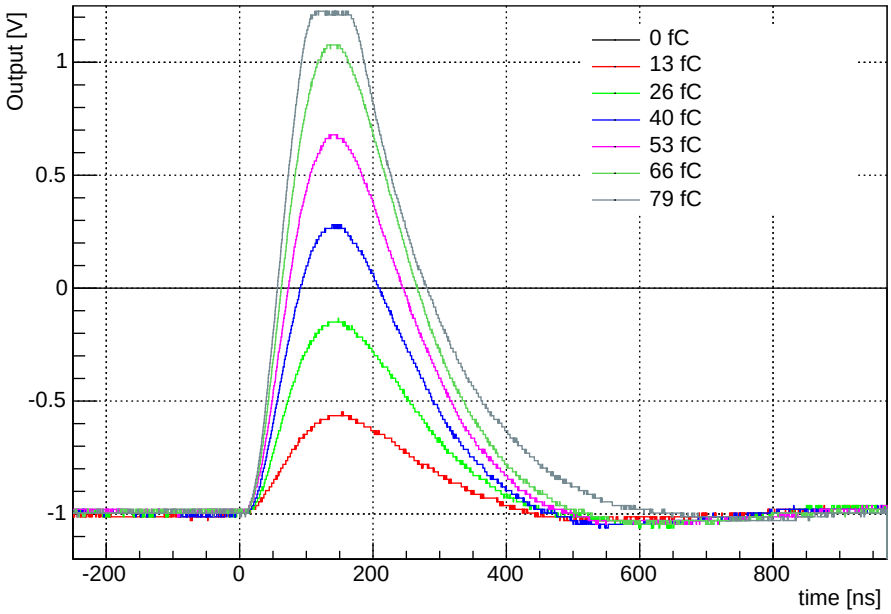

Figure 2. Front-end output pulses varying the injected charge for the 30mV/fC configuration.

compatible results. The response of the front-end is linear, with residual less than 10 mV, (non linearity < 0.5% of the full range) till above 90% of the range. The figure 3 shows a typical response curve. The sensitivity was found close to the nominal values. The spread among different channels and different chips was below 5%. The cross-talk was studied too. It was found to be up to 1%, but the presence of the effect even between non-neighbour channels indicated that the problem was in the reference voltage distribution, which was promptly corrected in the design of the next version of the circuit.

The Equivalent Noise Charge (ENC) was calculated measuring the signal rms value in absence of an injected charge. To improve the measurement precision, it was considered the average value over 1000 measurements. The oscilloscope and its probe were adding noise whose amplitude was of the same order of magnitude of circuit under test. This contribution was estimated by taking measurements with the chip turned off, and then removed quadratically from the value measured with the chip on. The dependency of the noise on the detector capacitance was measured adding several values of pre-calibrated capacitances between the input and the ground. While one channel was being measured, each of the other four channels inputs were connected to a 22 pF capacitor to ground, simulating the pad detector.

Figure 4 shows the noise vs capacitance curve for different chips/channels, from the different laboratories. The solid line is the simulation result while the points represents the experimental values, that start at 15 pF due to the parasitic capacitance coming from the package and from the board traces and connectors.

The chip was tested mainly powering it at nominal voltage, 1.25 V, but several tests were performed also at the lowest (1.19 V) and at the highest (1.31 V) limit. Operating at lower voltage does not show any alteration in the chip behaviour, besides reducing the dynamic range. When operated at the higher voltage the chip behave well, too, with the exception of the 30 mV/fC,

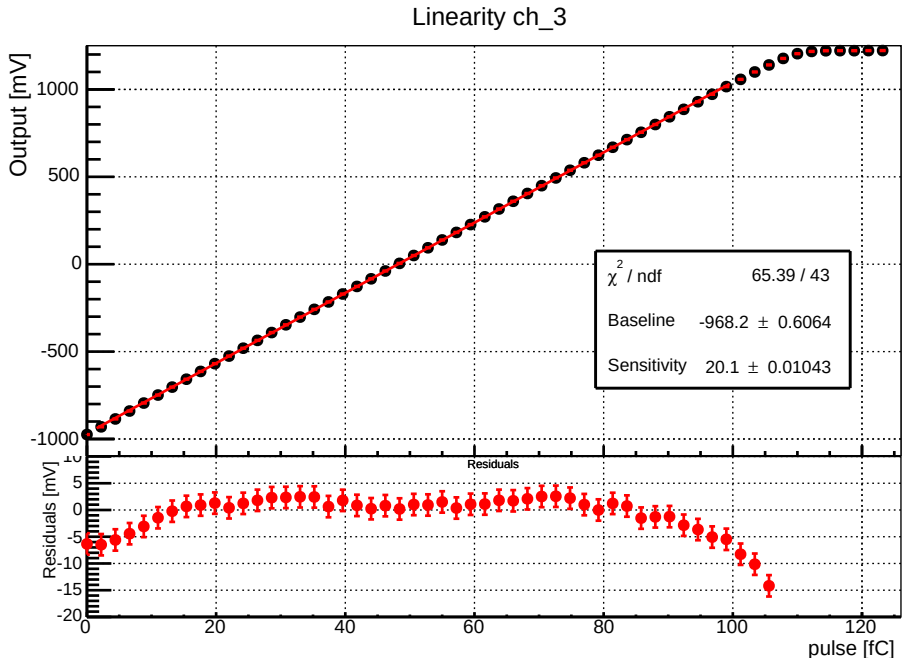

Figure 3. A calibration curve for the configuration 20mV/fC.

negative charge pulse, configuration. In this configuration many chip/channels showed instability. Eventually the effect was reproduced and understood in simulation: the layout implemented in this prototype was introducing a parasitic coupling between output and input, which, for negative charge configuration, was resulting in a positive feedback. That was corrected for the next version.

3.2 Characterising the ADC

The chip_2, containing a 10 bit SAR ADC circuit and a prototype of the SLVS transmitter and receiver drivers, measured $\approx$ 2x2 mm^2. The circuit, especially in this stand-alone prototype, is sensitive to the series inductance on the reference voltage line. For this reason the ADC was tested mounting directly the bare die on the test-board, taking care of keeping the bonding wires length as short as possible and placing appropriate buffer capacitors on the board. The ADC was operated at the nominal frequency of 10 MHz, provided by an external function generator. The power consumption resulted lower than 1.5mW. The 10 bits output was read out as a parallel word by a FPGA. First the ADC was stimulated with different type of slow varying (10 kHz) signals, like ramp, sine wave (figure 5, left), etc., looking for evident problems of no-linearity or/and missing codes. Later a sine wave with frequency values ranging from 400 kHz till 4.7 MHz was used, and SINAD, SFDR and ENOB were computed. The equivalent number of bits, measured at 2.031250 MHz, resulted of 9.38 (figure 5, right). Similar values were obtained when measured at the others stimulus frequencies.

4 Conclusions

The SAMPA ASIC is being designed to attend the needs for a new faster readout of the Time Projection Chamber and Muon Chambers of the ALICE experiment and a first prototype was measured and validated.

2016 JINST 11 C02088

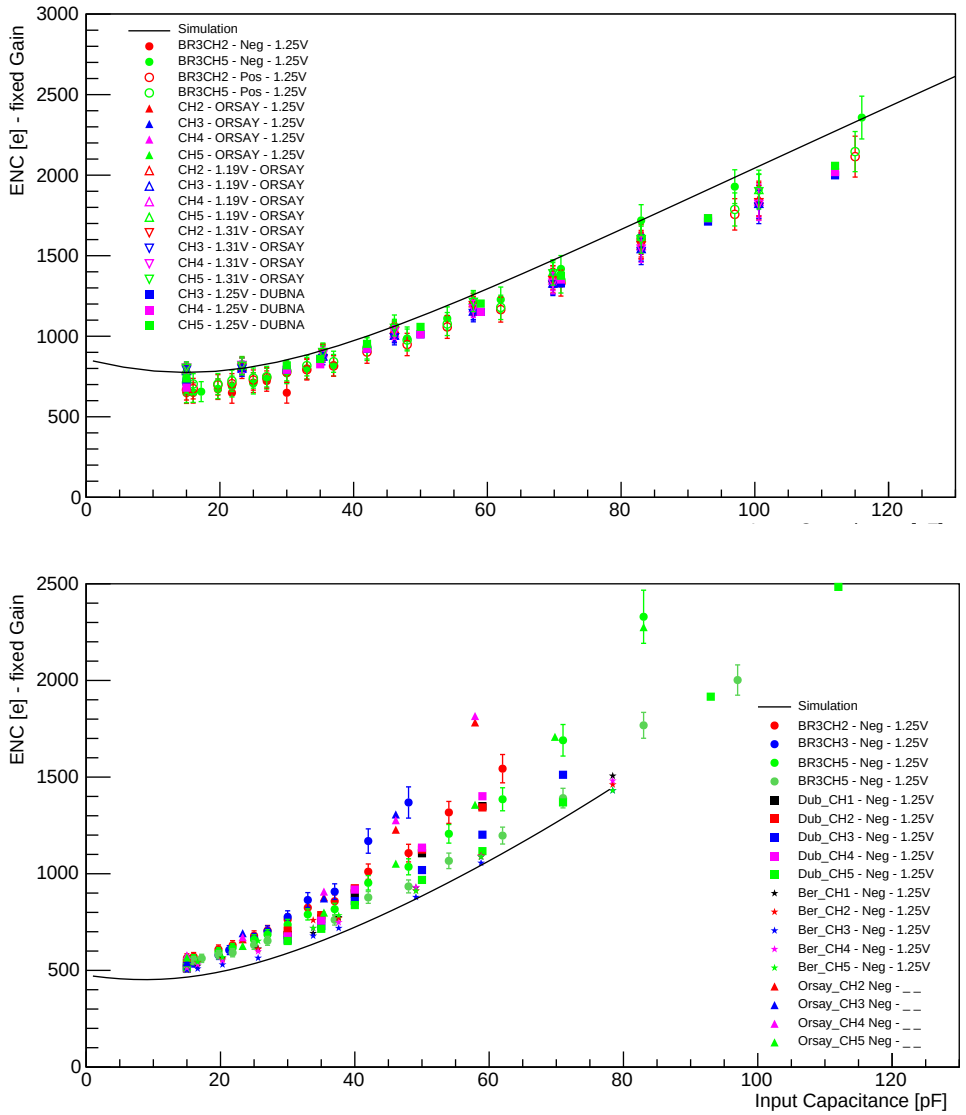

Figure 4. Noise, expressed in ENC, for 4mV/fC (top) and 20mV/fC (bottom) configurations in various chips/channels, measured by the different laboratories. ENC was calculated using nominal gain.

The Front-End part (CSA followed by two shaper stages) proved to work properly and reasonably close to the specifications for both high gain (20 and 30 mV/fC with 160 ns shaping) and low gain (4 mV/fC, 300 ns shaping) configuration. Some limitations were discovered, whose cause was understood and already corrected in the design of the new prototype.

The tests of the standalone 10 bit SAR ADC block demonstrated the circuit could reach an ENOB figure of ≈ 9.2 bits or better, provided the reference voltages are maintained stable. This is addressing special cautions in the final design of the full chip

The next step consists in designing and producing a full size (32 channels) prototype, integrating the front-end, the ADC, a complete DSP and several SLVS links.

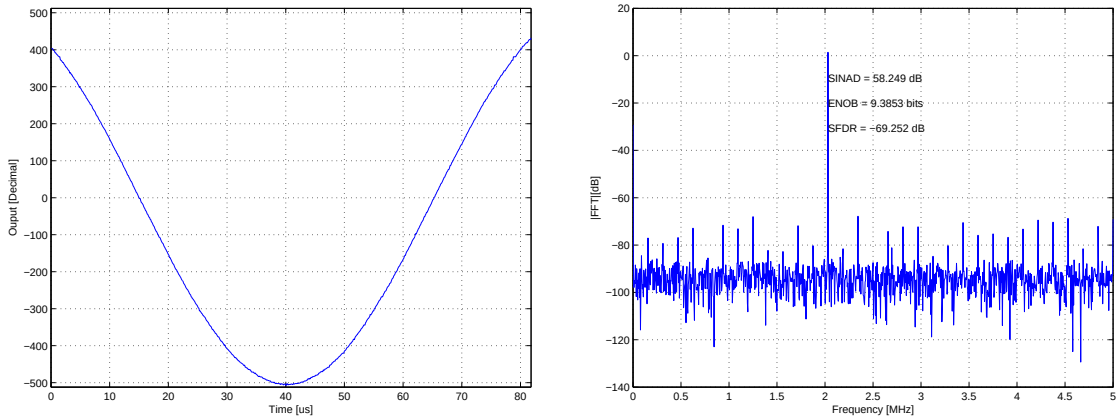

Figure 5. Measured performance of SAMPA_MPW1 ADC: output in response a 10 kHz sine wave input (left), ADC spectrum in presence of 2MHz sine wave (right).

Acknowledgments

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2016 JINST 11 C02088